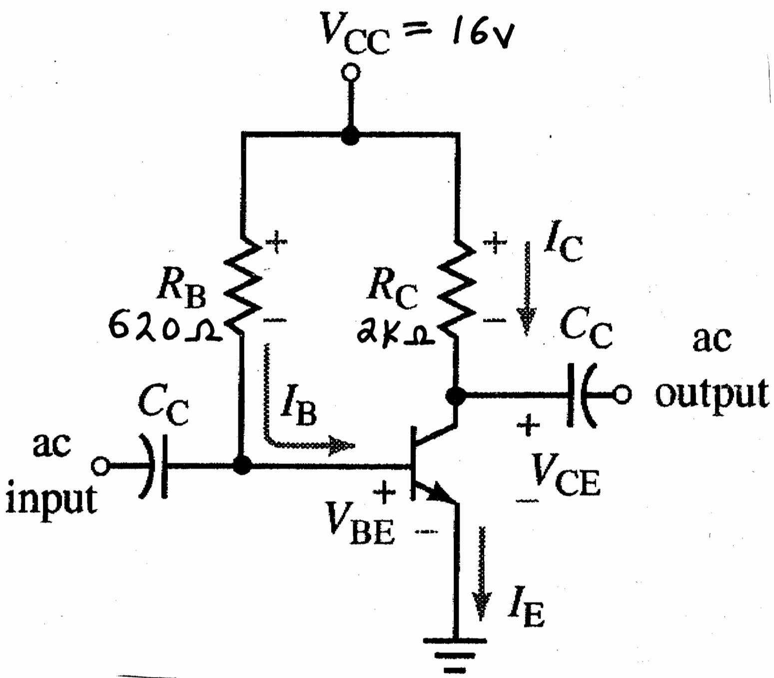
(21) $\beta = 120 \leftarrow \frac{I_C}{I_B}$

ANSWERS
CH 28: 21, 31, 43 & 45.



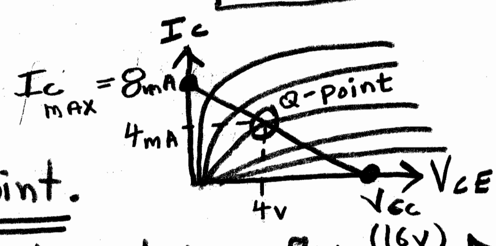
(a) "Saturation" means
- I_c is at max.
- $V_{CE} \approx 0\,V$.

Since $V_{CE} = 0$,

$V_{R_c} = V_{cc} = 16v$

So, $I_{c_{SAT}} = \frac{V_{Rc}}{R_c} = \frac{16v}{2K\Omega}$

$= \boxed{8\,mA}$



(b) Find I_B, I_c, I_E and V_{CE} at Q-point.
Q-point is located in middle $\Rightarrow V_Q \approx \frac{1}{2} V_{cc} = 8v$

$\Rightarrow I_c \approx \frac{1}{2} I_{c_{MAX}} = 4mA$

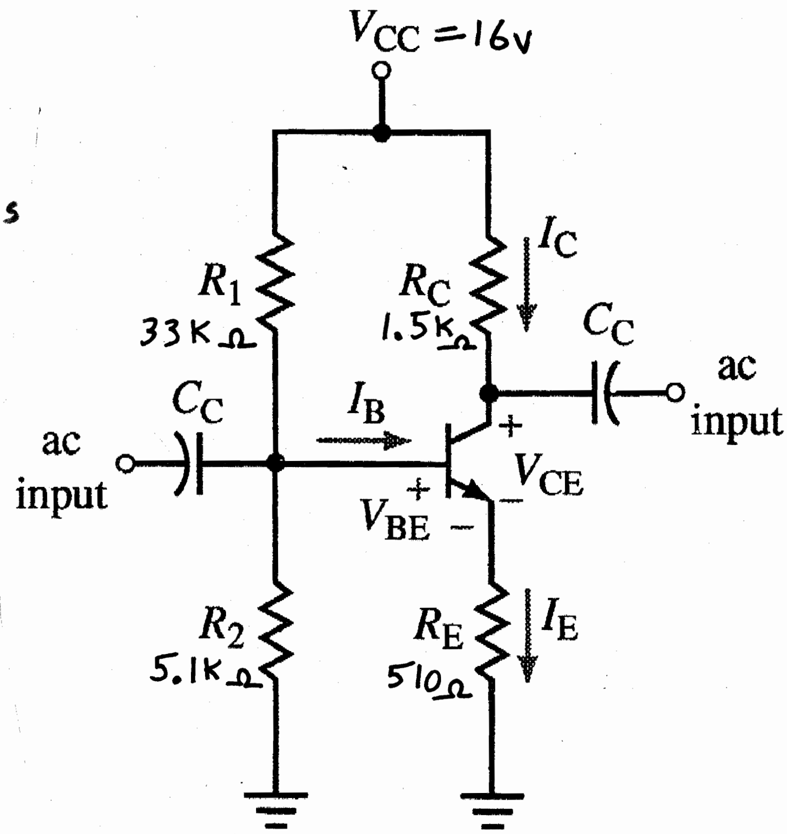
So, $\boxed{V_{CE} = 4v}$ and $\boxed{I_c = 4mA}$.

$I_B = \frac{I_c}{120} = \frac{4\,mA}{120} = \boxed{33\mu A}$

$I_E = I_c + I_B = 4\,mA + 33\mu A = \boxed{4.033\,mA}$

(c) See load line here — — — —

(31) $\beta = 120$



(a) "Saturation" means that $V_{CE} \approx 0$.

$\Rightarrow V_{cc}$ (16v) drops across $R_c + R_E$

$$\Rightarrow I_{c_{SAT}} = \frac{V_{cc}}{R_c + R_E} = \frac{16v}{1.5k + 510}$$

$$\boxed{= 7.96mA}$$
$$\boxed{\approx 8mA}$$

(b) Solve for I_B, I_c, I_E & V_{CE} at Q-point.

Endpoints of load line are $I_{c_{MAX}} = I_{c_{SAT}} = 8mA$

and $V_{CE} = V_{cc} = 16v$

Q-point is in middle $\Rightarrow V_{CE_{Qpt}} = \frac{1}{2} V_{cc} = \boxed{8v}$

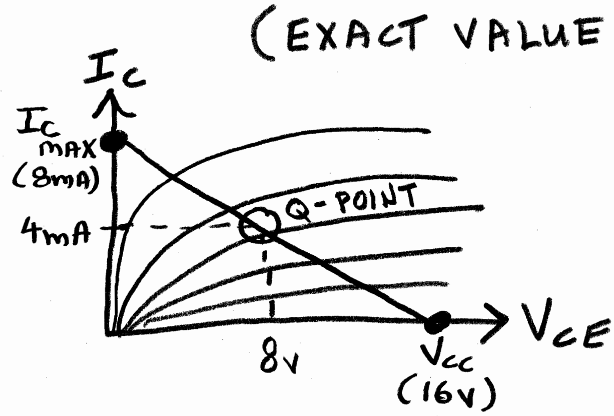
$$I_{c_{Qpt}} = \frac{1}{2} I_{c_{MAX}} = \boxed{4mA}$$

$$I_B = \frac{I_c}{\beta} = \frac{4mA}{120} = \boxed{33\mu A}$$

$$I_E = I_c + I_B = 4mA + 33\mu A = \boxed{4.033mA}$$

(EXACT VALUE $= 3.98mA + 33\mu A$
$= 4.013\ mA$)

(c)



(43) **NOTE:** Problem says $R_c = 470\,\Omega$, but diagram says $430\,\Omega$. I will use the $470\,\Omega$ value.

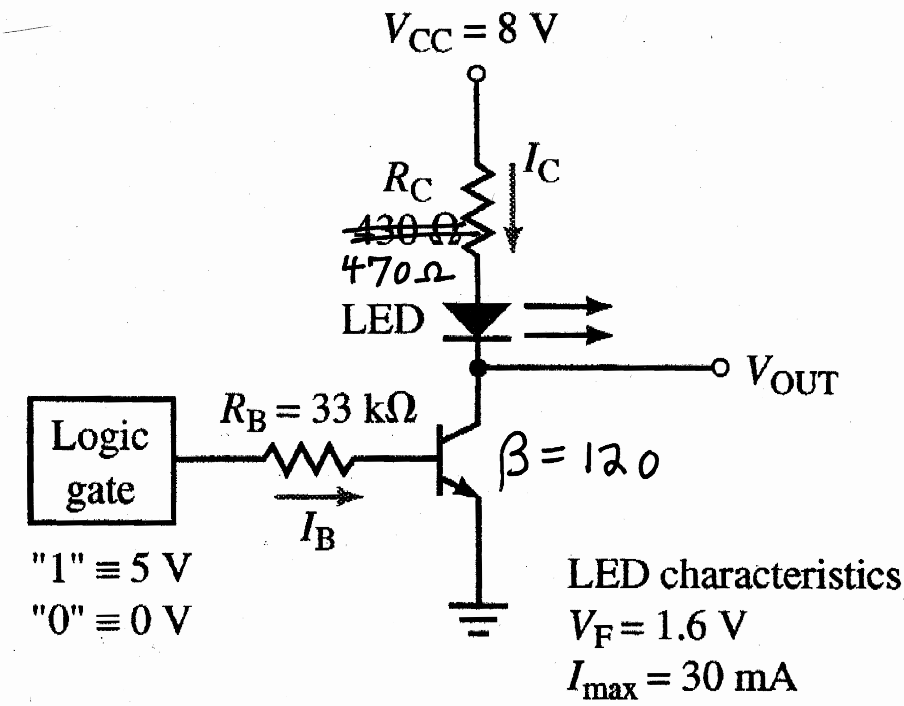
(a) $I_{c_{SAT}} = I_{c_{MAX}}$

Remember that "saturation" means $V_{CE}=0$.

$\Rightarrow$ V_{cc} drops across only R_c and the LED.

$\Rightarrow V_{R_c} = V_{cc} - V_{LED}$
$= 8v - 1.6v$
$= 6.4v$

$\Rightarrow I_c = \dfrac{6.4v}{470\,\Omega}$
$= \boxed{13.6mA}$



(b) If Logic gate is Logic 1 $\Rightarrow$ Transistor is ON.
$\Rightarrow$ Transistor saturated.
$\Rightarrow V_{CE} = 0$

$V_{R_c} = 8v - V_F$
$= 8v - 1.6v = 6.4v$

$I_c = \dfrac{V_{Rc}}{R_c} = \dfrac{6.4v}{470\,\Omega} = \boxed{13.6mA}$

(c) In Part (a), transistor is saturated. $\Rightarrow V_c = V_{CE} = \boxed{0v}$

(d) Logic gate at Logic 0 $\Rightarrow$ Transistor is OFF.
$\Rightarrow I_c = 0 \Rightarrow I_{LED} = \boxed{0A}$

(e) In (d) $I_c = 0 \Rightarrow V_{OUT}$ floats to $V_{cc} = \boxed{+8v}$

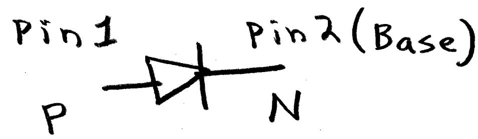
(45) Pin 1(+) Pin 2(−) ⇒ 0.223 kΩ ⇒ Conducts.
Pin 2(+) Pin 1(−) ⇒ ∞ Ω ⇒ No conduction.

Pin 2 (+) Pin 3(−) ⇒ ∞ Ω ⇒ No conduction.
Pin 3 (+) Pin 2 (−) ⇒ 0.259 kΩ ⇒ Conducts.

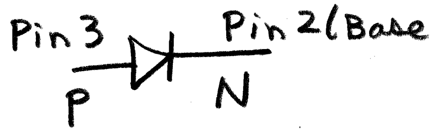
Pin 1 (+) Pin 3(−) ⇒ ∞ Ω
Pin 3(+) Pin 1 (−) ⇒ ∞ Ω
} MUST BE OUTER PINS ⇒ C and E

<u>Step 1</u>: Pins that give ∞ both ways are the outer (C and E) connections.
⇒ Know that 2 <u>must</u> be the <u>Base</u>.

<u>Step 2</u>: Pin 1 (+) Pin 2(−) conducts.
⇒ Pin 1 must be P-type and Pin 2 must be N-type.



<u>Step 3</u>: Pin 3(+) Pin 2(−) conducts.
⇒ Similar to Pins 1 & 2.



(a) Thus Pin 3 − Pin 2 − Pin 1 are **P−N−P.**

(b) Pin 2 is Base. Pins 1 & 3 are C & E, but do <u>not</u> know which is which!